IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

XMTT, INC., Plaintiff, v. INTEL CORPORATION, Defendant.	Civil Action No. _____ **JURY TRIAL DEMANDED**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff XMTT, Inc. ("XMTT"), by and through its undersigned counsel, brings this action for patent infringement against Intel Corporation ("Intel"), and alleges as follows:

THE PARTIES

1. Plaintiff XMTT is a corporation duly organized and existing under the laws of the State of Delaware, having its principal place of business at 3 Kettle Pond Ct., Potomac, MD 20854.

2. XMTT is the assignee and owns all right, title, and interest to U.S. Patent Nos. 8,145,879 ("the '879 Patent") and 7,707,388 ("the '388 Patent") (collectively, the "Asserted Patents").

3. On information and belief, Defendant Intel is a corporation duly organized and existing under the laws of the State of Delaware, having its principal place of business at 2200 Mission College Blvd., Santa Clara, CA 95054.

JURISDICTION AND VENUE

4. This is an action arising under the patent laws of the United States, 35 U.S.C. § 1 *et seq.* Accordingly, this Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

5. This court has personal jurisdiction over Intel because Intel is incorporated in Delaware. Intel also, among other things, manufactures products that are and have been used, offered for sale, sold, and purchased in the District of Delaware.

6. Under 28 U.S.C. §§ 1391(b)-(d) and 1400(b), venue is proper in this judicial district because, among other things, Intel is incorporated in Delaware and thus resides in this judicial district.

FIRST CLAIM

(Infringement of U.S. Patent No. 8,145,879)

7. XMTT re-alleges and incorporates herein by reference Paragraphs 1-6 of its Complaint.

8. The '879 Patent, entitled "Computer Memory Architecture For Hybrid Serial And Parallel Computing Systems," was duly and lawfully issued March 27, 2012. A true and correct copy of the '879 Patent is attached hereto as Exhibit 1.

9. The '879 Patent names Uzi Y. Vishkin as inventor. Dr. Vishkin is a professor at the University of Maryland in the Department of Electrical and Computer Engineering. He was selected as a Fellow in the Association of Computing Machinery in 1996 for, among other things, having "played a leading role in forming and shaping what thinking in parallel has come to mean in the fundamental theory of Computer Science." Dr. Vishkin has hundreds of published papers in the field of parallel computing and computer architecture and is a frequent invited speaker at academic conferences and within the computer hardware industry, including at Intel's research and development facilities.

10. The ’879 Patent has been in full force and effect since its issuance. XMTT owns by assignment the entire right, title, and interest in and to the ’879 Patent, including the right to seek damages for past, current, and future infringement thereof.

11. The ’879 Patent states that it “generally relate[s] to computing and more specifically to a computer memory architecture for hybrid serial and parallel computing systems.” Ex. 1 at 1:32-34.

12. The ’879 Patent explains that “parallelism has provided a growing opportunity for increased performance of computer systems,” but that “in many applications, however, it is necessary to perform both serial and parallel processing.” Ex. 1, at 1:35-42. The ’879 Patent further explains that “conventional approaches often do not allow for efficient execution of coordinated, mixed (i.e., ‘hybrid’) parallel and serial processing modes,” creating a need for the patented technology. Ex. 1 at 1:52-61.

13. The ’879 Patent provides, in one embodiment, “a serial processor [that] is configured to execute software instructions in a software program in serial. A serial memory is configured to store data for use by the serial processor in executing the software instructions in serial. A plurality of parallel processors are configured to execute software instructions in the software program in parallel. A plurality of partitioned memory modules are provided and configured to store data for use by the plurality of parallel processors in executing software instructions in parallel. Accordingly, a processor/memory structure is provided that allows serial programs to use quick local serial memories and 40 parallel programs to use partitioned parallel memories.” Ex. 1, at 3:30-41. The ’879 Patent further explains that the parallel processors may include “read-only cache” memory. Ex. 1, at 5:9-15.

14. The systems and methods taught by the '879 Patent solve discrete, technological problems associated with the architecture of multicore computing systems, representing new, novel and useful improvements over the existing and/or patentably distinct means and methods. The '879 Patent claims describe particular computer hardware components, such as processors and memory, organized in a particular way and with particular functionality that improves the capabilities, such as speed and power efficiency, of a computer processing system. For example, the '879 Patent describes systems and methods that provide more "efficient execution of coordinated, mixed (i.e., 'hybrid') parallel and serial processing modes" as compared to "conventional approaches." Ex. 1, at 1:52-61. The '879 Patent's improvements to computer systems are further described in its specification.

15. XMTT is informed and believes, and thereon alleges, that Intel has infringed and unless enjoined will continue to infringe one or more claims of the '879 Patent, in violation of 35 U.S.C. § 271, by, among other things, making, using, offering to sell, and selling within the United States, supplying or causing to be supplied in or from the United States, and importing into the United States, without authority or license, Intel products that infringe claims of the '879 Patent, including Intel products containing Intel® Graphics Technology.

16. The '879 accused products, for example, embody every limitation of at least claim 1 of the '879 Patent, literally or under the doctrine of equivalents, as set forth below. The further descriptions below, which are based on publicly available information, are preliminary examples and are non-limiting.

[<u>**"An apparatus comprising: a serial processor to execute instructions in a computing program primarily in serial;"**</u>**]**

17. The '879 accused products include systems-on-a-chip (or "SoCs"), which comprise one or more serial processors ("CPU cores") to execute instructions in a computing program primarily in serial, as described, for example, in Intel's technical specification "The Compute Architecture of Intel Processor Graphics Gen9" ("Gen9 Specification").

18. The SoC architecture for Intel Core-series processors, for instance, is illustrated on page 3 of the Gen9 Specification.

4 SoC Architecture

This section describes the SoC architecture within which Intel processor graphics is a component.

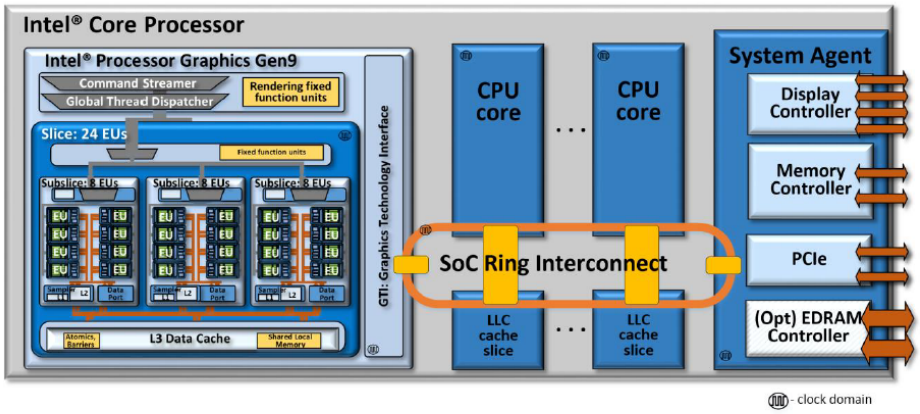


Figure 2: An Intel® Core™ i7 processor 6700K SoC and its ring interconnect architecture.

19. The specification illustrates, for example, that the '879 accused products include, among other hardware components, at least one "CPU core" (serial processor). The CPU core(s) execute computer programs, which are comprised of instructions, primarily in serial.

["a first, private memory to store data solely for use by the serial processor in executing the instructions;"]

20. In the Intel architectures used in the '879 accused products, CPU cores have at least one private memory to store data solely for use by the CPU cores in executing the program instructions. For example, as described in Intel's Introduction to Intel® Architecture White Paper, in an exemplary quad-core Intel Core i7 processor, "the four CPUs each ha[ve] [their] own L1 and

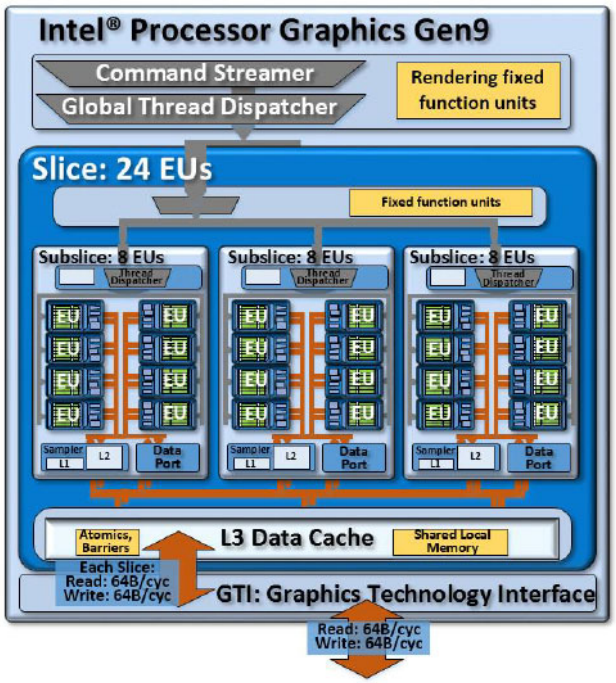
L2 caches."

https://www.intel.com/content/dam/www/public/us/en/documents/white-papers/ia-introduction-basics-paper.pdf at 5. These cache memories store data that is solely for use by the CPU core in executing program instructions.

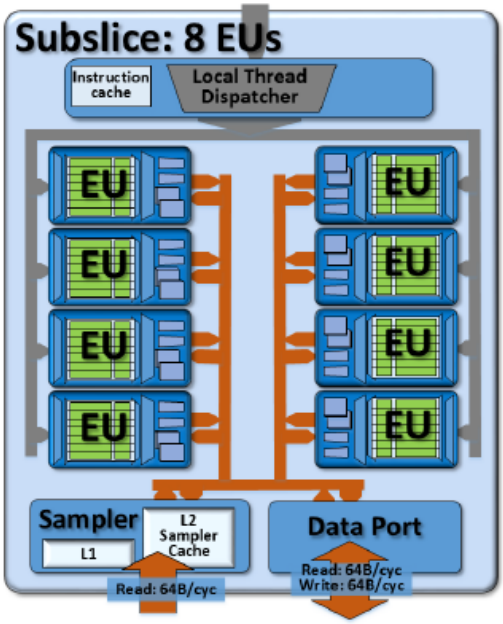
["a plurality of parallel processors to execute instructions in the computing program primarily in parallel, at least one parallel processor of the plurality of parallel processors having a second, local read-only memory; and"]

21. The graphics hardware in the '879 accused products comprises a plurality of parallel processors to execute instructions in the computing program primarily in parallel, at least one parallel processor of the parallel processors having a second, local read-only memory.

22. For example, the diagram at page 13 of the Gen9 Specification illustrates the components of Intel's graphics architecture, including one or more Slices, each of which is comprised of a plurality of Subslices, each of which further comprises, among other components, a plurality of Execution Units.



23. By way of further example, each Subslice is also a parallel processor that executes instructions in a computing program primarily in parallel. As illustrated in the figure on page 9 of the Gen9 Specification, for instance, each Subslice has its own local thread dispatcher, and multiple parallel execution units.



24. Each Subslice also contains a "sampler," as illustrated in the figure above. Intel's Gen9 Specification explains that the "sampler is a **read-only memory** fetch unit."

["a plurality of shared memory modules to store data for use by the plurality of parallel processors in executing the instructions."]

25. The '879 accused products further comprise a plurality shared memory modules to store data for use by the plurality of parallel processors in executing the instructions.

26. As illustrated above, for example, each graphics Slice contains an L3 Data Cache memory that is shared by that Slice's plurality of parallel processors. The L3 Data Cache acts as "shared local memory" for use in executing the program instructions. Gen9 Specification, at 11.

Intel products with multiple Subslices "instantiate multiple L3 cache partitions," which "aggregate together via an L3 fabric and act as a single larger capacity monolithic cache." *Id.*

27. Intel has had actual knowledge of its infringement of the '879 Patent since at least the time of service of this Complaint, and continues to infringe the '879 Patent notwithstanding that knowledge. XMTT is further informed and believes that Intel has had actual knowledge of its infringement of the '879 Patent since before the time of service of this Complaint, including for the reasons that, for example: Intel has been well aware of the research of Dr. Uzi Vishkin, the sole inventor of the '879 Patent, into multicore architectures and parallelism for many years, including Dr. Vishkin's work with his company, XMTT, the original assignee of the '879 Patent and Plaintiff in this action – indeed, in recent correspondence with Dr. Vishkin regarding a potential collaboration, an Intel engineer remarked that "we [Intel] have known your early work on XMT and as you may recall we had invited you to Intel a few years back." The Intel engineer was correct. In fact, on multiple occasions, including in 2008, while the Asserted Patents were pending, in 2010, shortly after the '388 Patent issued, and again in 2013, shortly after the '879 Patent issued, Intel considered investing in XMTT or otherwise acquiring Dr. Vishkin's intellectual property. Intel instead chose to release multiple generations of infringing products without permission. As a further example of Intel's extensive knowledge of Dr. Vishkin's work, on multiple occasions, Dr. Vishkin was invited to Intel's facilities to discuss, and did discuss, his Explicit Multi-Threading (XMT) technology associated with the Asserted Patents. For example, over the years Dr. Vishkin has given numerous technical presentations to Intel's chip architects, including, for example: in 2008, at Intel's China Research Center in Beijing, China; in 2009, at Intel's Israel Development Center in Haifa, Israel; in 2010, in a videotaped talk on parallel programming that was broadcast on Intel Software Network TV; in 2012, as part of the

Distinguished Speaker Series at the Illinois-Intel Parallelism Center (broadcast throughout Intel); and again at Intel's Haifa facility in 2015 and 2017. During these presentations, Dr. Vishkin described key technical aspects of his patented technologies and informed Intel at the time that the technologies were protected by U.S. patents issued and pending. Dr. Vishkin also provided Intel, on multiple occasions, with links to his XMT website, where he has maintained a list of issued U.S. patent numbers related to his XMT technologies (including the Asserted Patents). In addition to invited talks, Dr. Vishkin has given numerous presentations on his patented technologies at industry conferences attended by Intel personnel, including, for example, the 2010 Indo-US Conference on Parallelism in Bangalore, India, where Dr. Vishkin's presentation included a slide referencing "6 Issued Patents" and "More patent applications" (which, at the time, included the parent application to the '879 Patent). Dr. Vishkin has also identified the Asserted Patents in widely-read published papers, including, for example, in "Algorithmic Approach to Designing an Easy-To-Program System: Can It Lead to a HW-Enhanced Programmer's Workflow Add-On?," which was published in the proceedings of the 2009 IEEE International Conference on Computer Design and describes U.S. Patent Application No, 2009/0119481 (the published application of the parent of the '879 Patent) as "show[ing] how to gracefully upgrade from a uniprocessor to up to thousands of processors on-chip without losing on backwards compatibility on serial code, and dynamically moving back and forth between serial and parallel execution." Intel not only attended, presented multiple papers, and chaired the first conference session of the 2009 IEEE conference, but also received (as special session chair) an advance copy of Dr. Vishkin's paper before the conference. As a further example, Dr. Vishkin's paper "Using Simple Abstraction to Reinvent Computing for Parallelism," which was published in the Communications of the ACM magazine in January 2011, references issued patents related to the XMT processor, including the '388 Patent

(parent to the '879 Patent, which was at the time a published pending patent application). This paper has been downloaded over 19,000 times from the ACM Digital Library and was referenced in the first slide of Dr. Vishkin's presentation at the Illinois-Intel Parallelism Center, which was broadcast throughout Intel. Furthermore, as previously mentioned, Dr. Vishkin has maintained a website for his XMT technology which includes, among other things, a detailed description of Dr. Vishkin's technologies and a list of related U.S. patents (including the '879 Patent) by number. Intel is, and has been, well aware of Dr. Vishkin's XMT website. For example, an Intel engineer provided a quote for publication on the XMT website praising Dr. Vishkin's technical accomplishments, and, as noted above, Dr. Vishkin has informed Intel of his XMT website on numerous occasions over the years. As a further example, Intel architects have touted the benefits of Dr. Vishkin's XMT technology to Intel's customers within Intel's own Developer Zone (an online forum for discussion of Intel products), specifically referencing Dr. Vishkin's XMT website. To the extent Intel claims it did not have actual knowledge of the '879 Patent, particularly in light of the foregoing, Intel has been willfully blind to that patent's existence based on, for example, its publicly-known corporate policy forbidding its employees from reading patents held by outside companies or individuals.

28. XMTT is informed and believes, and thereon alleges, that Intel actively, knowingly, and intentionally has induced infringement of the '879 Patent by, for example, controlling the design and manufacture of, offering for sale, selling, supplying, and otherwise providing instruction and guidance regarding the above-described products with the knowledge and specific intent to encourage and facilitate infringing uses of such products by its customers both inside and outside the United States (as used in this pleading, "customers" refers to both direct and indirect customers, including entities that distribute and resell the accused products, alone or as part of a

system, and end users of such products and systems). For example, Intel publicly provides documentation, including datasheets available through Intel's publicly accessible ARK service and software developer's manuals, instructing customers on uses of Intel's products that infringe the '879 Patent. *See, e.g.*, http://ark.intel.com. On information and belief, Intel's customers directly infringe the '879 Patent by, for example, making, using, offering to sell, and selling within the United States, and importing into the United States, without authority or license, products containing the above-described Intel products, and/or supplying or causing to be supplied from the United States all or a substantial portion of the components of such products, where such components are uncombined in whole or in part, in such manner as to actively induce, as described above, the combination of such components outside the United States in a manner that would infringe the '879 Patent if such combination occurred inside the United States.

29. XMTT is informed and believes, and thereon alleges, that Intel has contributed to the infringement by its customers of the '879 Patent by, without authority, importing, selling and offering to sell within the United States materials and apparatuses for practicing the claimed invention of the '879 Patent both inside and outside the United States. For example, the above-described products constitute a material part of the inventions of the '879 Patent and are not staple articles or commodities of commerce suitable for substantial noninfringing use. On information and belief, Intel knows that the above-described products constitute a material part of the inventions of the '879 Patent and are not staple articles or commodities of commerce suitable for substantial noninfringing use. On information and belief, Intel's customers directly infringe the '879 Patent by, for example, making, using, offering to sell, and selling within the United States, and importing into the United States, without authority or license, products containing the above-described Intel products, and/or supplying or causing to be supplied from the United States

components of such products that are especially made or especially adapted for use in the inventions of the ’879 Patent and not a staple article or commodity of commerce suitable for substantial noninfringing use, where such components are uncombined in whole or in part, knowing, as described above, that such components are so made or adapted intending that such components will be combined outside the United States in a manner that would infringe the ’879 Patent if such combination occurred inside the United States.

30. As a result of Intel’s infringement of the ’879 Patent, XMTT has been damaged. XMTT is entitled to recovery for damages sustained as a result of Intel’s wrongful acts in an amount subject to proof at trial.

31. To the extent 35 U.S.C. § 287 is determined to be applicable, on information and belief, its requirements have been satisfied with respect to the ’879 Patent.

32. In addition, Intel’s infringing acts and practices have caused and are causing immediate and irreparable harm to XMTT.

33. XMTT is informed and believes, and thereon alleges, that the infringement of the ’879 Patent by Intel has been and continues to be willful. As noted above, Intel has had knowledge of the ’879 Patent, or, at minimum, has been willfully blind to the existence of the ’879 Patent. Intel has deliberately continued to infringe in a wanton, malicious, and egregious manner, with reckless disregard for XMTT’s patent rights. Thus, Intel’s infringing actions have been and continue to be consciously wrongful.

34. XMTT is informed and believes, and thereon alleges, that this is an exceptional case, which warrants an award of attorney’s fees to XMTT pursuant to 35 U.S.C. § 285.

SECOND CLAIM

(Infringement of U.S. Patent No. 7,707,388)

35. XMTT re-alleges and incorporates herein by reference Paragraphs 1-34 of its Complaint.

36. The ’388 Patent, entitled “Computer Memory Architecture For Hybrid Serial And Parallel Computing Systems,” was duly and lawfully issued April 27, 2010. A true and correct copy of the ’388 Patent is attached hereto as Exhibit 2.

37. The ’388 Patent names Uzi Y. Vishkin as inventor. Dr. Vishkin is a professor at the University of Maryland in the Department of Electrical and Computer Engineering. He was selected as a Fellow in the Association of Computing Machinery in 1996 for, among other things, having “played a leading role in forming and shaping what thinking in parallel has come to mean in the fundamental theory of Computer Science.” Dr. Vishkin has hundreds of published papers in the field of parallel computing and computer architecture and is a frequent invited speaker at academic conferences and within the computer hardware industry, including at Intel’s research and development facilities.

38. The ’388 Patent has been in full force and effect since its issuance. XMTT owns by assignment the entire right, title, and interest in and to the ’388 Patent, including the right to seek damages for past, current, and future infringement thereof.

39. The ’388 Patent states that it “generally relate[s] to computing and more specifically to a computer memory architecture for hybrid serial and parallel computing systems.” Ex. 2, at 1:25-27.

40. The ’388 Patent explains that “parallelism has provided a growing opportunity for increased performance of computer systems,” but that “in many applications, however, it is

necessary to perform both serial and parallel processing." Ex. 2, at 1:28-35. The '388 Patent further explains that "conventional approaches often do not allow for efficient execution of coordinated, mixed (i.e., 'hybrid') parallel and serial processing modes," creating a need for the patented technology. Ex. 2, at 1:45-54.

41. The '388 Patent provides, in one embodiment, "a serial processor [that] is configured to execute software instructions in a software program in serial. A serial memory is configured to store data for use by the serial processor in executing the software instructions in serial. A plurality of parallel processors are configured to execute software instructions in the software program in parallel. A plurality of partitioned memory modules are provided and configured to store data for use by the plurality of parallel processors in executing software instructions in parallel. Accordingly, a processor/memory structure is provided that allows serial programs to use quick local serial memories and 40 parallel programs to use partitioned parallel memories." Ex. 2, at 3:22-33. The '388 Patent further explains that in particular embodiments, "a serial processor controls transitions from a serial processing mode to a parallel processing mode implemented by a plurality of parallel processors." Ex. 2, at 2:1-3.

42. The systems and methods taught by the '388 Patent solve discrete, technological problems associated with the architecture of multicore computing systems, representing new, novel and useful improvements over the existing and/or patentably distinct means and methods. The '388 Patent claims describe particular computer hardware components, such as processors and memory, organized in a particular way and with particular functionality that improves the capabilities, such as speed and power efficiency, of a computer processing system. For example, the '388 Patent describes systems and methods that provide more "efficient execution of coordinated, mixed (i.e., 'hybrid') parallel and serial processing modes" as compared to

"conventional approaches." Ex. 2, at 1:45-54. The '388 Patent's improvements to computer systems are further described in its specification.

43. XMTT is informed and believes, and thereon alleges, that Intel has infringed and unless enjoined will continue to infringe one or more claims of the '388 Patent, in violation of 35 U.S.C. § 271, by, among other things, making, using, offering to sell, and selling within the United States, supplying or causing to be supplied in or from the United States, and importing into the United States, without authority or license, Intel products that infringe claims of the '388 Patent, including Intel products containing Intel® Graphics Technology.

44. The '388 accused products, for example, embody every limitation of at least claim 1 of the '388 Patent, literally or under the doctrine of equivalents, as set forth below. The further descriptions below, which are based on publicly available information, are preliminary examples and are non-limiting.

["An apparatus comprising: a serial processor to execute software instructions in a software program primarily in serial;"]

45. The '388 accused products include systems-on-a-chip (or "SoCs"), which comprise one or more serial processors ("CPU cores") to execute software instructions in a computer program primarily in serial, as described, for example, in Intel's technical specification "The Compute Architecture of Intel Processor Graphics Gen9" ("Gen9 Specification") (available at https://software.intel.com/sites/default/files/managed/c5/9a/The-Compute-Architecture-of-Intel-Processor-Graphics-Gen9-v1d0.pdf).

46. The SoC architecture for Intel Core-series processors is illustrated, for instance, on page 3 of the Gen9 Specification.

4 SoC Architecture

This section describes the SoC architecture within which Intel processor graphics is a component.

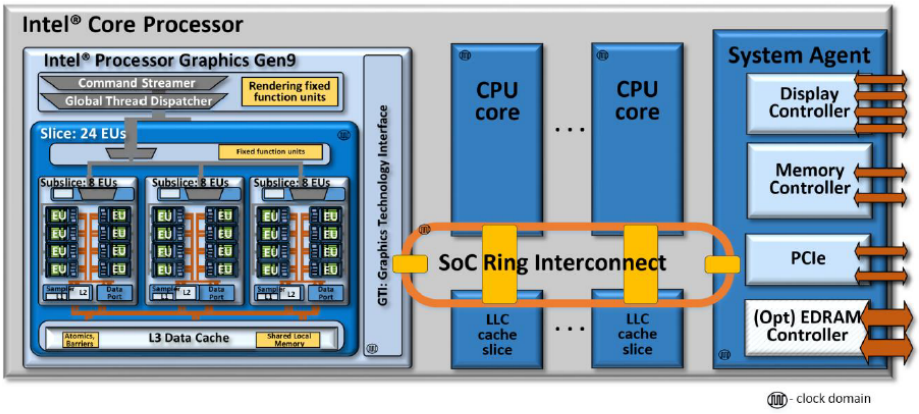


Figure 2: An Intel® Core™ i7 processor 6700K SoC and its ring interconnect architecture.

47. The specification illustrates, for example, that the '388 accused products include, among other hardware components, at least one "CPU core" (serial processor). The CPU core(s) execute computer programs, which are comprised of software instructions, primarily in serial.

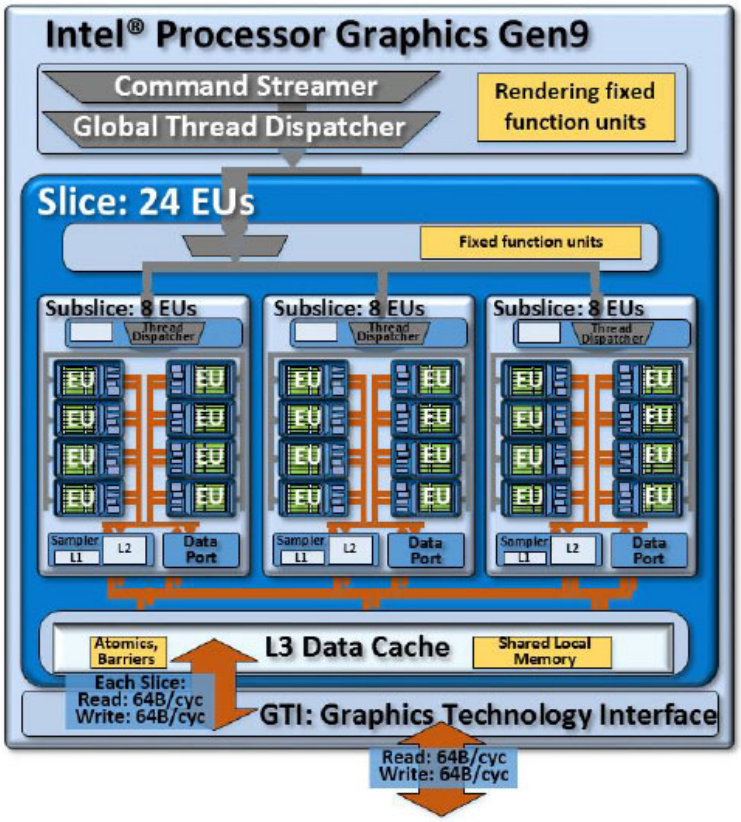
["a serial memory adapted to store data for use by the serial processor in executing the software instructions primarily in serial;"]

48. In the Intel architectures used in the '388 accused products, CPU cores have at least one serial memory adapted to store data for use by the CPU cores in executing the software instructions primarily in serial. For example, as described in Intel's Introduction to Intel® Architecture White Paper, in an exemplary quad-core Intel Core i7 processor, "the four CPUs each ha[ve] [their] own L1 and L2 caches." https://www.intel.com/content/dam/www/public/us/en/documents/white-papers/ia-introduction-basics-paper.pdf at 5. These cache memories store data for use by the serial CPU core in executing its software instructions.

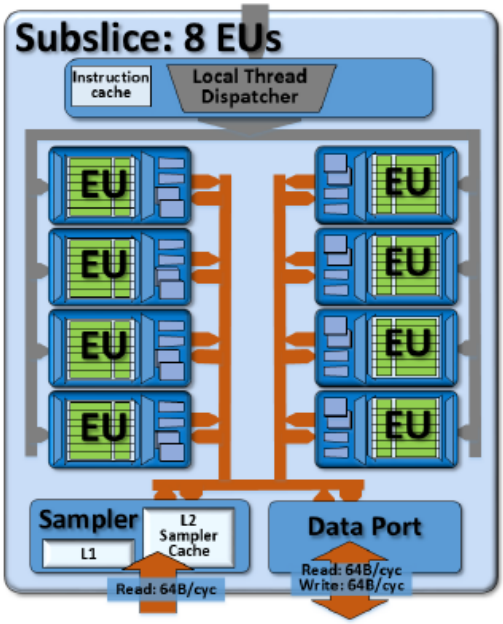
["a plurality of parallel processors adapted to execute software instructions in the software program primarily in parallel; and"]

49. The graphics hardware in the '388 accused products comprises a plurality of parallel processors adapted to execute software instructions in the computing program primarily in parallel.

50. For example, the diagram at page 13 of the Gen9 Specification illustrates the components of Intel's graphics architecture, including one or more Slices, each of which is comprised of a plurality of Subslices, each of which further comprises, among other components, a plurality of Execution Units.



51. By way of further example, each Subslice also executes instructions in a computing program primarily in parallel. As illustrated in the figure on page 9 of the Gen9 Specification, for example, each Subslice has its own instruction cache, local thread dispatcher, and multiple parallel execution units.



["a plurality of partitioned memory modules adapted to store data for use by the plurality of parallel processors in executing the software instructions primarily in parallel;"]

52. The '388 accused products further comprise a plurality of partitioned memory modules adapted to store data for use by the plurality of parallel processors in executing the software instructions primarily in parallel.

53. As illustrated above, for instance, each graphics Slice contains an L3 Data Cache memory that is shared by that Slice's plurality of parallel processors. The L3 Data Cache acts as "shared local memory" for use in executing the program instructions. Gen9 Specification, at 11. Intel products with multiple Subslices "instantiate multiple L3 cache partitions," which "aggregate together via an L3 fabric and act as a single larger capacity monolithic cache." *Id.*

["wherein the serial processor is further adapted, prior to a transition from a serial processing mode to a parallel processing mode, to provide for a transfer of updated data from the serial memory to at least one of the plurality of partitioned memory

modules and to receive a corresponding acknowledgement from the at least one of the plurality of partitioned memory modules that the updated data has been queued or committed prior to any memory requests from the plurality of parallel processors."]

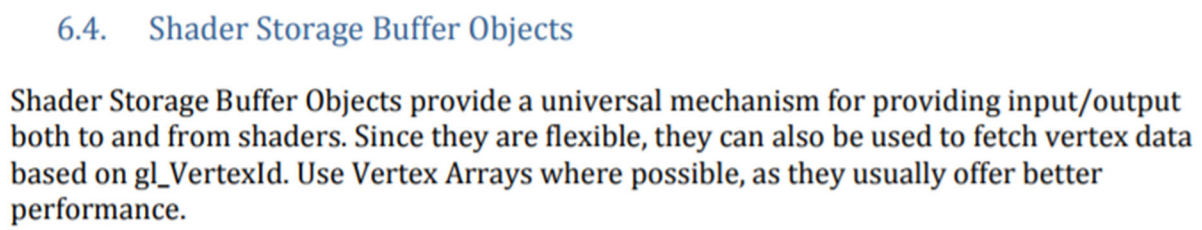
54. In the '388 accused products, a transition from a serial processing mode to a parallel processing mode occurs, for example, when the software program running on the CPU cores dispatches a computing task to the graphics hardware for processing in parallel. For example, a software program may use the OpenGL 4.5 library function "glDispatchCompute" to cause a transition from a serial processing mode to a parallel processing mode." https://www.khronos.org/registry/OpenGL-Refpages/gl4/ at glDispatchCompute. As another example, a software program running on the CPU cores may invoke a "shader" program designed to execute on the graphics hardware. Intel's hardware is designed to be compatible with software libraries, including OpenGL and Microsoft Direct3D, and Intel provides documentation instructing users how to use these libraries with the '388 accused products. *See, e.g.*, https://software.intel.com/sites/default/files/managed/3a/93/6th-gen-graphics-api-dev-guide-1.1.pdf at 5:

> This guide introduces the graphics hardware architecture of 6th gen Intel Core processors and provides expert tips and best practices to consider when leveraging their features and capabilities. The document also provides guidance and direction on how to get better performance from the newest graphical APIs running on Intel® Processor Graphics.
>
> In addition, you'll also find reference material for using the latest graphics APIs (Direct3D* 12 and OpenGL* 4.4), with occasional information on older APIs interwoven throughout. For full details on Direct3D 11, OpenGL 4.3, and earlier graphics API editions, as well as additional details on programming for earlier generations of Intel® processors, please see our online Processor Graphics document library.

55. The CPU cores in the '388 accused products are adapted to, prior to a transition from a serial processing mode to a parallel processing mode, provide for a transfer of updated data from the serial memory to at least one of the plurality of partitioned memory modules and to

receive a corresponding acknowledgement from the at least one of the plurality of partitioned memory modules that the updated data has been queued or committed prior to any memory requests from the plurality of parallel processors.

56. For example, updated data is transferred from the CPU cores to the partitioned memory modules accessible by the plurality of parallel processors using buffer objects, as described in Intel technical documentation such as the specification included below.



6.4. Shader Storage Buffer Objects

Shader Storage Buffer Objects provide a universal mechanism for providing input/output both to and from shaders. Since they are flexible, they can also be used to fetch vertex data based on gl_VertexId. Use Vertex Arrays where possible, as they usually offer better performance.

https://software.intel.com/sites/default/files/managed/3a/93/6th-gen-graphics-api-dev-guide-1.1.pdf at 36.

57. These buffer objects must be successfully allocated and the data committed to the partitioned memory modules before any memory requests can be made by the plurality of parallel processors, *e.g.*, to execute graphics processing instructions. *See, e.g.*, https://www.khronos.org/opengl/wiki/Buffer_Object ("Buffer objects hold a linear array of memory of arbitrary size. This memory must be allocated before it can be uploaded to or used."); https://www.khronos.org/opengl/wiki/Vertex_Specification#Vertex_Array_Object ("A Vertex Array Object (VAO) is an OpenGL Object that stores all of the state needed to supply vertex data (with one minor exception noted below). It stores the format of the vertex data as well as the Buffer Objects (see below) providing the vertex data arrays."); https://www.khronos.org/opengl/wiki/Vertex_Rendering ("The following represent conditions you must ensure are valid when issuing a drawing command. A non-zero Vertex Array Object

must be bound (though no arrays have to be enabled, so it can be a freshly-created vertex array object).").

58. Intel has had actual knowledge of its infringement of the '388 Patent since at least the time of service of this Complaint, and continues to infringe the '388 Patent notwithstanding that knowledge. XMTT is further informed and believes that Intel has had actual knowledge of its infringement of the '388 Patent since before the time of service of this Complaint, including for the reasons that, for example: Intel has been well aware of the research of Dr. Uzi Vishkin, the sole inventor of the '388 Patent, into multicore architectures and parallelism for many years, including Dr. Vishkin's work with his company, XMTT, the original assignee of the '388 Patent (and Plaintiff in this action) – indeed, in recent correspondence with Dr. Vishkin regarding a potential collaboration, an Intel engineer remarked that "we [Intel] have known your early work on XMT and as you may recall we had invited you to Intel a few years back." The Intel engineer was correct. In fact, on multiple occasions, including in 2008, while the Asserted Patents were pending, in 2010, shortly after the '388 Patent issued, and again in 2013, shortly after the '879 Patent issued, Intel considered investing in XMTT or otherwise acquiring Dr. Vishkin's intellectual property. Intel instead chose to release multiple generations of infringing products without permission. As a further example of Intel's extensive knowledge of Dr. Vishkin's work, on multiple occasions, Dr. Vishkin was invited to Intel's facilities to discuss, and did discuss, his Explicit Multi-Threading (XMT) technology that is associated with the Asserted Patents. For example, over the years Dr. Vishkin has given numerous technical presentations to Intel's chip architects, including, for example: in 2008, at Intel's China Research Center in Beijing, China; in 2009, at Intel's Israel Development Center in Haifa, Israel; in 2010, in a videotaped talk on parallel programming that was broadcast on Intel Software Network TV; in 2012, as part of the

Distinguished Speaker Series at the Illinois-Intel Parallelism Center (broadcast throughout Intel); and again at Intel's Haifa facility in 2015 and 2017. During these presentations, Dr. Vishkin described key technical aspects of his patented technologies and informed Intel at the time that the technologies were protected by U.S. patents issued and pending. Dr. Vishkin also provided Intel, on multiple occasions, with links to his XMT website, where he has maintained a list of issued U.S. patent numbers related to his XMT technologies (including the Asserted Patents). In addition to invited talks, Dr. Vishkin has given numerous presentations on his patented technologies at industry conferences attended by Intel personnel, including, for example, the 2010 Indo-US Conference on Parallelism in Bangalore, India, where Dr. Vishkin's presentation included a slide referencing "6 Issued Patents" and "More patent applications" (which, at the time, included the publicly-available patent application that would issue as the '388 Patent approximately three months later). Dr. Vishkin has also identified the Asserted Patents in widely-read published papers, including, for example, in "Algorithmic Approach to Designing an Easy-To-Program System: Can It Lead to a HW-Enhanced Programmer's Workflow Add-On?," which was published in the proceedings of the 2009 IEEE International Conference on Computer Design and describes U.S. Patent Application No, 2009/0119481 (the published application of the '388 Patent) as "show[ing] how to gracefully upgrade from a uniprocessor to up to thousands of processors on-chip without losing on backwards compatibility on serial code, and dynamically moving back and forth between serial and parallel execution." Intel not only attended, presented multiple papers, and chaired the first conference session of the 2009 IEEE conference, but also received (as special session chair) an advance copy of Dr. Vishkin's paper before the conference. As a further example, Dr. Vishkin's paper "Using Simple Abstraction to Reinvent Computing for Parallelism," which was published in the Communications of the ACM magazine in January 2011, references issued

patents related to the XMT processor, including the '388 Patent. This paper has been downloaded over 19,000 times from the ACM Digital Library and was referenced in the first slide of Dr. Vishkin's presentation at the Illinois-Intel Parallelism Center, which was broadcast throughout Intel. Furthermore, as previously mentioned, Dr. Vishkin has maintained a website for his XMT technology which includes, among other things, a detailed description of Dr. Vishkin's technologies and a list of related U.S. patents (including the '388 Patent) by number. Intel is, and has been, well aware of Dr. Vishkin's XMT website. For example, an Intel engineer provided a quote for publication on the XMT website praising Dr. Vishkin's technical accomplishments, and, as noted above, Dr. Vishkin has informed Intel of his XMT website on numerous occasions over the years. As a further example, Intel architects have touted the benefits of Dr. Vishkin's XMT technology to Intel's customers within Intel's own Developer Zone (an online forum for discussion of Intel products), specifically referencing Dr. Vishkin's XMT website. To the extent Intel claims it did not have actual knowledge of the '388 Patent, particularly in light of the foregoing, Intel has been willfully blind to that patent's existence based on, for example, its publicly-known corporate policy forbidding its employees from reading patents held by outside companies or individuals.

59. XMTT is informed and believes, and thereon alleges, that Intel actively, knowingly, and intentionally has induced infringement of the '388 Patent by, for example, controlling the design and manufacture of, offering for sale, selling, supplying, and otherwise providing instruction and guidance regarding the above-described products with the knowledge and specific intent to encourage and facilitate infringing uses of such products by its customers both inside and outside the United States (as used in this pleading, "customers" refers to both direct and indirect customers, including entities that distribute and resell the accused products, alone or as part of a system, and end users of such products and systems). For example, Intel publicly provides

documentation, including datasheets available through Intel's publicly accessible ARK service and software developer's manuals, instructing customers on uses of Intel's products that infringe the '388 Patent. *See, e.g.*, http://ark.intel.com. On information and belief, Intel's customers directly infringe the '388 Patent by, for example, making, using, offering to sell, and selling within the United States, and importing into the United States, without authority or license, products containing the above-described Intel products, and/or supplying or causing to be supplied from the United States all or a substantial portion of the components of such products, where such components are uncombined in whole or in part, in such manner as to actively induce, as described above, the combination of such components outside the United States in a manner that would infringe the '388 Patent if such combination occurred inside the United States.

60. XMTT is informed and believes, and thereon alleges, that Intel has contributed to the infringement by its customers of the '388 Patent by, without authority, importing, selling and offering to sell within the United States materials and apparatuses for practicing the claimed invention of the '388 Patent both inside and outside the United States. For example, the above-described products constitute a material part of the inventions of the '388 Patent and are not staple articles or commodities of commerce suitable for substantial noninfringing use. On information and belief, Intel knows that the above-described products constitute a material part of the inventions of the '388 Patent and are not staple articles or commodities of commerce suitable for substantial noninfringing use. On information and belief, Intel's customers directly infringe the '388 Patent by, for example, making, using, offering to sell, and selling within the United States, and importing into the United States, without authority or license, products containing the above-described Intel products, and/or supplying or causing to be supplied from the United States components of such products that are especially made or especially adapted for use in the

inventions of the ’388 Patent and not a staple article or commodity of commerce suitable for substantial noninfringing use, where such components are uncombined in whole or in part, knowing, as described above, that such components are so made or adapted intending that such components will be combined outside the United States in a manner that would infringe the ’388 Patent if such combination occurred inside the United States.

61. As a result of Intel’s infringement of the ’388 Patent, XMTT has been damaged. XMTT is entitled to recovery for damages sustained as a result of Intel’s wrongful acts in an amount subject to proof at trial.

62. To the extent 35 U.S.C. § 287 is determined to be applicable, on information and belief, its requirements have been satisfied with respect to the ’388 Patent.

63. In addition, Intel’s infringing acts and practices have caused and are causing immediate and irreparable harm to XMTT.

64. XMTT is informed and believes, and thereon alleges, that the infringement of the ’388 Patent by Intel has been and continues to be willful. As noted above, Intel has had knowledge of the ’388 Patent, or, at minimum, has been willfully blind to the existence of the ’388 Patent. Intel has deliberately continued to infringe in a wanton, malicious, and egregious manner, with reckless disregard for XMTT’s patent rights. Thus, Intel’s infringing actions have been and continue to be consciously wrongful.

65. XMTT is informed and believes, and thereon alleges, that this is an exceptional case, which warrants an award of attorney’s fees to XMTT pursuant to 35 U.S.C. § 285.

PRAYER FOR RELIEF

WHEREFORE, XMTT prays for judgment against Intel as follows:

A. That Intel has infringed, and unless enjoined will continue to infringe, each of the Asserted Patents;

B. That Intel has willfully infringed each of the Asserted Patents;

C. That Intel pay XMTT damages adequate to compensate XMTT for Intel's infringement of the Asserted Patents, together with interest and costs under 35 U.S.C. § 284;

D. That Intel be ordered to pay prejudgment and postjudgment interest on the damages assessed;

E. That Intel pay XMTT enhanced damages pursuant to 35 U.S.C. § 284;

F. That Intel be ordered to pay supplemental damages to XMTT, including interest, with an accounting, as needed;

G. That Intel be enjoined from infringing the Asserted Patents, or if its infringement is not enjoined, that Intel be ordered to pay ongoing royalties to XMTT for any postjudgment infringement of the Asserted Patents;

H. That this be adjudged an exceptional case under 35 U.S.C. § 285, and that Intel pay XMTT's attorneys' fees, costs, and expenses in this action; and

I. That XMTT be awarded such other and further relief, including equitable relief, as the Court deems just and proper.

DEMAND FOR JURY TRIAL

Pursuant to Federal Rule of Civil Procedure 38(b), XMTT hereby demands a trial by jury on all issues triable to a jury.

Dated: November 16, 2018

Respectfully submitted,

FARNAN LLP

/s/ *Brian E. Farnan*

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